



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/615,077

07/08/2003

Steven C. Johnson

10017415-1

7949

22879

7590

11/18/2004

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER

NGUYEN, DANG T

ART UNIT

PAPER NUMBER

2824

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/615,077	Applicant(s) JOHNSON ET AL.	
	Examiner Dang T Nguyen	Art Unit 2824	
	-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --		

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 27 September 2004.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-44 is/are pending in the application.

4a) Of the above claim(s) _____ is/are ~~with~~ drawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-44 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 08 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892) 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6) <input type="checkbox"/> Other: _____.
---	--

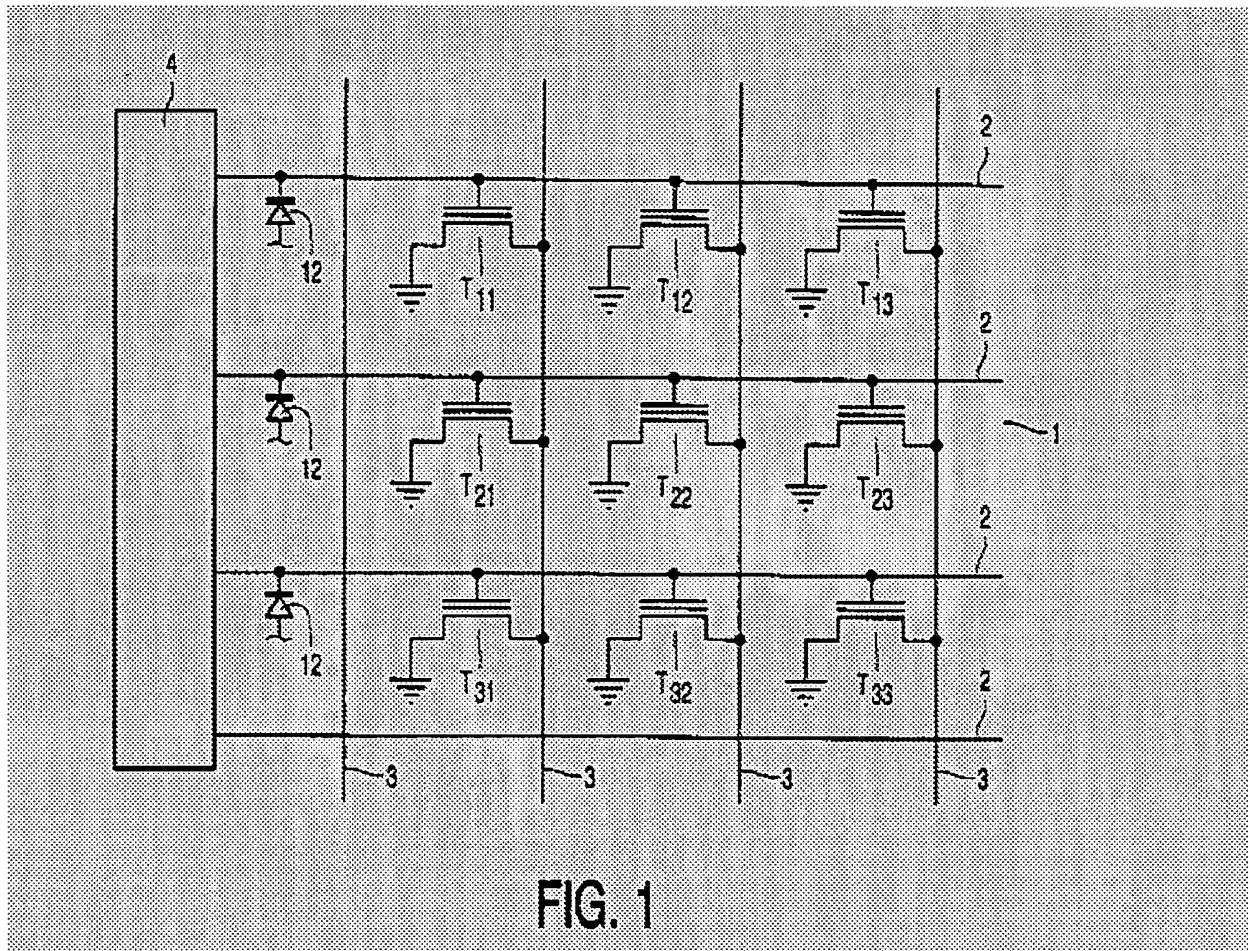
DETAILED ACTION

1. This office action is in response to applicant's amendment filed on 09/23/04. Claims 1, 30, 32, 33, 34, and 35 have been amended. Claims 36 – 44 have been added. Claims 1, 5, 10, 30, 32, 33, 34, 35, 36, 41, and 43 are independent claims. Claims 1 – 44 are pending on this application.

Response to Arguments

2. Applicant's arguments filed 09/23/04 have been fully considered but they are not persuasive.

First, applicant noted that Widdershoven does not disclose or suggest a high-density non-volatile fast memory "having no erasing circuitry" as is required by claim 1 (under Remark, page 10 line 19 – page 11 line 1), applicant pointed to photodiode 12 in Fig. 1 of Widdershoven (6,313,502) that generates a photo-voltage during UV irradiation of the memory cell to prevent under-erasure of the memory cell. Therefore, Widdershoven fails to teach a memory having no erasing circuitry. Examiner respectful disagrees from the following:



Col. 4 lines 49 – 53, Widdershoven discloses the photodiode 12 is using to prevent under erasure during UV irradiation. Widdershoven clearly teaches the photodiode 12 does not perform any erasure, in addition photodiode 12 is using to preventing erasure. Therefore, photodiode 12 is not an erasing circuitry. As is described Fig. 1 and Fig. 2 of Widdershoven clearly teaches a high-density non-volatile flash memory having no erasing circuitry, see Fig. 2 below

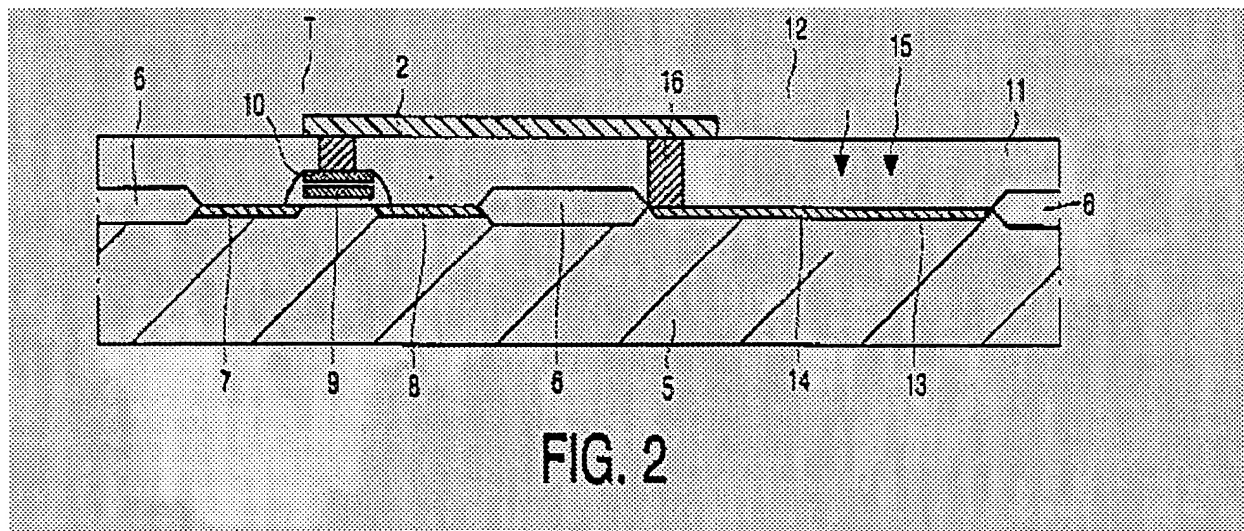


Fig. 2 of Widdershoven discloses the UV radiation [15] is used to erase the flash cell (Col. 1 lines 10-11); therefore, no erasing circuitry in the flash memory.

Second, with respect to claims 3 and 5 (under Remarks, page 11, lines 6-13) applicant argued that Widdershoven does not disclose "two terminal drain-gate-connected modified flash cells having no erasing circuitry" Widdershoven's memory cell is three terminal memory. Examiner respectfully disagrees from the following:

Fig. 1 of Widdershoven clearly teaches a modified flash cell (11) by UV light having two terminals drain [2] and gate [3]. Therefore, Widdshoven clearly anticipated the two terminals (drain [2] and gate [3]) comprised by the memory cell of claimed invention.

Third, with respect to claims 10, 30, 34, and 35 (under Remarks, page 11 line 14 – page 12 line 2), Widdershoven does not discloses "modified flash cells having no erasing circuitry". Examiner respectfully disagrees for the same reasons discussed above in relation to claim 1.

Fourth, with respect to claims 33 and 35 (under Remarks, page 12 lines 7 – page 13 line 1) applicant noted that Kazami does not explicitly disclose “erasing the non-volatile memory by exposing the non-volatile memory to the UV light through the UV light windows without the use of any erasing circuitry”, examiner respectfully disagrees because Col.1 lines 14 – 18, Kazami et al. clearly teaches an erasing the non-volatile memory (EPROM) by exposing the non-volatile memory to the UV light through the UV light windows without using of any erasing circuitry.

Fifth, with respect to claim 4 (under Remark, page 13 lines 8-12), examiner respectfully disagrees for the same reasons discussed above in relation to claim 1. Claim 4 is clearly unpatentable over Widdershoven in view of Maayan et al.

Sixth, with respect to claims 7 - 8, 16 - 17, 19 - 20, and 22 – 23 (under remark, page 13 lines 18-23), examiner respectfully disagrees for the same reasons discussed above in relation to claims 5 and 10. Claims 7 - 8, 16 - 17, 19 - 20, and 22 – 23 are clearly unpatentable over Widdershoven in view of Wu.

Seventh, with respect to claims 25 – 29 (under remark, page 14 lines 6-10), examiner respectfully disagrees for the same reasons discussed above in relation to claims 5 and 10. Claims 25 - 29 are clearly unpatentable over Widdershoven in view of Wu.

Eight, with respect to claim 31 (under remark, page 14 lines 16-17), examiner respectfully disagrees for the same reasons discussed above in relation to claim 30 above (the same reasons discussed in relation to claim 1). Claim 31 is clearly unpatentable over Widdershoven in view of Kozicki.

Per discussed above, the prior arts from previous office action is applied to this office action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-6, 9-15, 18, 21, 24, 30, 32, 34, 36-37, and 40-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Widdershoven, U.S. Patent No. 6,313,502 B1 – filed Nov. 30, 1999.

Regarding independent claim 1, Widdershoven discloses a system comprising: a high-density non-volatile fast memory (Col. 1 line 10) having no erasing circuitry (Col. 1 line 10, [Widdershoven teaches using UV light to erase memory cells, therefore, no erasing circuitry in the flash memory]); and an ultraviolet (UV) light window adapted to expose the high-density non-volatile fast memory to UV light (Col. 1 lines 10-12 and 35-37).

Regarding dependent claim 2, Widdershoven discloses wherein the high-density non-volatile fast memory comprises a modified flash memory having no erasing circuitry (Col. 1 line 10, [Widdershoven teaches using UV light to erase memory cells, therefore, no erasing circuitry in the flash memory]).

Regarding dependent claim 3, Figs. 1 and 2 of Widdershoven discloses wherein the high-density non-volatile fast memory comprises a two-terminal drain-gate-connected modified flash cell having no erasing circuitry (Col. 1 lines 10-16).

Regarding independent claim 5, Widdershoven discloses a device comprising: two-terminal drain-gate-connected modified flash cells having no erasing circuitry (Col. 1 lines 10-16); and an ultraviolet (UV) light window adapted to expose the two-terminal drain-gate-connected modified flash cells to UV light (Col. 1 lines 10-12 and 35-37).

Regarding dependent claim 6, Figs. 1 and 2 of Widdershoven discloses wherein the two-terminal drain-gate-connected modified flash cells are configured as a two-dimensional planar matrix of cells (Col. 3 lines 54-56 and Col. 4 lines 5-7).

Regarding dependent claim 9, Fig. 2 of Widdershoven discloses wherein the two-terminal drain-gate-connected modified flash cells are configured as three-dimensional layers (Col. 1 lines 10-16).

Regarding independent claim 10, Widdershoven discloses a system comprising: modified flash cells having no erasing circuitry (Col. 1 line 10, [Widdershoven teaches using UV light to erase memory cells, therefore, no erasing circuitry in the flash memory]); and an ultraviolet (UV) light window adapted to expose the modified flash cells to UV light (Col. 1 lines 10-12 and 35-37).

Regarding dependent claim 11, Fig. 2 of Widdershoven discloses wherein the UV light window [15] is located above a control gate [10] of the modified flash cells.

Regarding dependent claim 12, Fig. 2 of Widdershoven discloses wherein the UV light window [15] is located below a substrate of the modified flash cells.

Regarding dependent claim 13, Fig. 4 of Widdershoven discloses wherein the UV light window is interposed between control gates of the modified flash cells.

Regarding dependent claim 14, Widdershoven discloses wherein the UV light window is offset from control gates of the modified flash cells (Col. 4 lines 52-55).

Regarding dependent claim 15, Widdershoven discloses wherein the UV light window is adapted to diffuse UV light entering the UV light window (Col. 4 lines 45-49).

Regarding dependent claim 18, Figs. 1 and 2 of Widdershoven discloses wherein the modified flash cells are configured as a two-dimensional planar matrix of cells (Col. 3 lines 54-56 and Col. 4 lines 5-7).

Regarding dependent claim 21, Fig. 2 of Widdershoven discloses wherein the modified flash cells are configured as three-dimensional layers (Col. 1 lines 10-16).

Regarding dependent claim 24, Widdershoven further comprising an electronic device adapted to house the modified flash cells, the electronic device having an opening to receive the UV light window (Col. 1 lines 6-16).

Regarding independent claims 30 and 32, Widdershoven discloses a method comprising: exposing a modified and a high-density non-volatile fast memory to ultraviolet (UV) light (Col. 1 lines 35-37); and erasing the modified and the high-density non-volatile fast memory using the UV light (Col. 1 lines 9-12) without the use of any erasing circuitry (Col. 1 line 10, [Widdershoven teaches using UV light to erase memory cells, therefore, no erasing circuitry in the flash memory]).

Regarding independent claim 34, Widdershoven discloses a system comprising: means for exposing a modified flash cell to ultraviolet (UV) light (Col. 1 lines

35-37); and means for erasing the modified flash cell using the UV light without the use of any erasing circuitry (Col. 1 line 10, [Widdershoven teaches using UV light to erase memory cells, therefore, no erasing circuitry in the flash memory]).

Regarding independent claim 36, Widdershoven discloses a device comprising: two-terminal drain-gate-connected modified flash cells having no erasing circuitry (Col. 1 lines 10-16); and an ultraviolet (UV) light window adapted to expose the two-terminal drain-gate-connected modified flash cells to UV light (Col. 1 lines 10-12 and 35-37).

Regarding dependent claim 37, Figs. 1 and 2 of Widdershoven discloses wherein the two-terminal drain-gate-connected modified flash cells are configured as a two-dimensional planar matrix of cells (Col. 3 lines 54-56 and Col. 4 lines 5-7).

Regarding dependent claim 40, Fig. 2 of Widdershoven discloses wherein the two-terminal drain-gate-connected modified flash cells are configured as three-dimensional layers (Col. 1 lines 10-16).

Regarding independent claim 41, Fig. 1 of Widdershoven discloses a system comprising: a non-volatile memory; and an ultraviolet (UV) light window (Fig. 2 [11]) adapted to expose the high-density non-volatile fast memory to UV light (Fig. 2 [15]), wherein the UV light window (Fig. 2 [11]) is located below a substrate (Fig.2 [16]) of the memory.

Regarding dependent claim 42, Widdershoven discloses wherein the UV light window is adapted to diffuse UV light entering the UV light window (Col. 5 lines 21-27).

Regarding independent claim 43, Fig. 1 of Widdershoven discloses a system comprising: a non-volatile memory; and an ultraviolet (UV) light window (Fig. 2 [11]) adapted to expose the high-density non-volatile fast memory to UV light (Fig. 2 [15]), wherein the UV light window (Fig. 2 [11]) is located below a substrate (Fig. 2 [2 and 16]) of the memory, wherein the UV light window (Fig. 2 [11]) is interposed between control gates of the modified flash cells (Col. 4 lines 22-26).

Regarding dependent claim 44, Widdershoven discloses wherein the UV light window (Fig. 2 [11]) is adapted to diffuse UV light (Fig. 2 [15]) entering the UV light window (Col. 5 lines 21-25).

Claims 33 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Kazami et al., U.S. Patent No. 5,159,433 – filed Apr. 18, 1990.

Regarding independent claim 33, Kazami et al. discloses a method comprising: installing ultraviolet (UV) windows onto portable electronic devices having non-volatile memory (Col. 1 lines 14-18); and passing UV light through the UV windows (Col. 1 lines 14-17); and erasing the non-volatile memory by exposing the non-volatile memory to UV light through the UV light windows (Col. 1 lines 16-18 and 35-37) without the use of any erasing circuitry (Col. 1 line 10, [Widdershoven teaches using UV light to erase memory cells, therefore, no erasing circuitry in the flash memory]).

Regarding independent claim 35, Kazami et al. discloses a system comprising: means for installing ultraviolet (UV) windows onto portable electronic devices having non-volatile memory (Col. 1 lines 14-18); and means for erasing the non-volatile

memory by exposing the non-volatile memory to UV light through the UV light windows (Col. 1 lines 16-18 and 35-37) without the use of any erasing circuitry (Col. 1 line 10, [Widdershoven teaches using UV light to erase memory cells, therefore, no erasing circuitry in the flash memory]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Widdershoven, U.S. patent No. 6, 313,502 B1 – filed Nov. 30, 1999 in view of Maayan et al., Pub. No. US 2004/0008541 A1 – Pub. Date: Jan. 15, 2004.

Regarding dependent claim 4, Widdershoven as applied to claim 3 above disclosed every aspect of applicant's claimed invention except for the two-terminal drain-gate-connected modified flash cell is a diode-connected nitrated read-only memory (NROM) cell.

Fig. 2B of Maayan discloses a flash cell is a NROM cell (page 4, paragraph [0048]).

Widdershoven and Maayan et al. are common subject matter for non-volatile memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated Maayan's NROM cell into

Widdershoven's drain-gate, since Maayan taught the benefit by pointing out that the NROM cell particularly suitable for multiple use chips (Page 3, paragraph [0032] lines 7-8).

Claims 7-8, 16-17, 19-20, 22-23, and 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Widdershoven, U.S. patent No. 6, 313,502 B1 – filed Nov. 30, 1999 in view of Wu, Pub. No. US 2003/0146465 A1 – Pub. Date: Aug. 7, 2003.

Regarding dependent claims 7-8, 16-17, 19-20, 22-23, and 38-39, Widdershoven as applied to claims 6, 10, 18, 21, and 37 above, disclosed every aspect of applicant's claimed invention except for the two-dimensional planar matrix of cells is a NAND and a NOR configuration.

Wu discloses a gate structure having a configuration of NAND and NOR type (Page 1, paragraph [0004]).

Widdershoven and Wu are common subject matter for flash memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated Wu's NAND and NOR type into Widdershoven's matrix for the purpose of using NAND type for having very high parasitic capacitances between the select-gate (word) line and control-gate line, and using NOR type for obtaining high speed programming (page 1 paragraph [0004]).

Claims 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Widdershoven, U.S. patent No. 6, 313,502 B1 – filed Nov. 30, 1999 in view of Lin, Pub. No. US 2003/0064564 A1 – Pub. Date: Apr. 3, 2003.

Regarding dependent claims 25-29, Widdershoven as applied to claim 24 above, disclosed every aspect of applicant's claimed invention except for wherein the electronic device is a portable electronic device, a cellular telephone, a personal digital assistant (PDA), an MP3 player, and a lap-top computer.

Lin discloses the portable electronic device is a portable electronic device, a cellular telephone, a personal digital assistant (PDA), an MP3 player, and a lap-top computer (Page 1, paragraph [0004] lines 17-23).

Widdershoven and Lin are common subject matter for flash memory cell. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated Lin's portable electronic device into Widdershoven's flash cell, since Lin taught the benefit by pointing out that portability of these electrical consumer product is strongly prioritized by consumers, the products' size must be minimal (Page 1, paragraph [0004] lines 21-23).

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Widdershoven, U.S. patent No. 6, 313,502 B1 – filed Nov. 30, 1999 in view of Kozicki et al., U.S. patent No. 6,084,796 – filed: Jan. 12, 1999.

Regarding dependent claim 31, Widdershoven as applied to claim 30 above, disclosed every aspect of applicant's claimed invention except for passing light through a UV light window.

Fig. 10B of Kozicki et al. discloses the UV light [110] enters sensor [100] through window [109] (Col. 17 lines 33-35).

Kozicki and Widdershoven are common subject matter for non-volatile memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Kozicki's UV light window into Widdershoven's UV light for the purpose of enhancing the ionization of the metal during growth or dissolution of dendrite and hence the time to grow or dissolve dendrite is reduced (Col. 17 lines 40-43).

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

6. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.


Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Application/Control Number: 10/615,077

Page 16

Art Unit: 2824

Dang Nguyen 11/12/2004


RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800